CLAIMS

1. A random number generating method using: a plurality of unit circuits each having a first and a second logic circuit formed into an identical shape through an identical fabrication process and an amplifier circuit for forming a binary signal by amplifying a noise superposed on the differential voltage of threshold voltages of the first and the second logic circuits; and a signal variation detecting circuit for forming an output signal in response to variation in any of a plurality of binary signals outputted from the plurality of unit circuits, wherein a plurality of binary signals outputted from the signal variation detecting circuit are combined to generate a random number.

2. The random number generating method as claimed in claim 1, wherein

the first and the second logic circuit and the amplifier circuit are formed by logic gate circuits each having a first and a second input,

the first input and output of the logic gate circuit corresponding to the first logic circuit are connected,

the first input of the logic gate circuit corresponding to the second logic circuit is connected to the commonly connected input and output of the logic gate circuit corresponding to the first logic circuit,

the amplifier circuit includes a plurality of

logic gate circuits whose first input and output are connected vertically, and

the operation control signal is supplied to the second input of the logic gate constituting the first logic circuit, the second logic circuit, and the amplifier circuit so as to set the plurality of units circuits to an operation state to generate a random number via the signal variation detecting circuit.

3. The random number generating method as claimed in claim 2, wherein the plurality of unit circuits are successively selected in response to an operation control signal formed by an order circuit and output signals of all the unit circuits are outputted serially so as to generate a 1-bit random number by the signal variation detecting circuit.

4. The random number generating method as claimed in claim 3, wherein the signal variation detecting circuit uses an exclusive logic circuit for receiving output signals serially outputted from the order circuit and an output signal preceding by one so as to generate the random number.

5. The random number generating method as claimed in claim 3, wherein output signals of all the unit circuits corresponding to the 1-bit random number is also used as a chip identification signal.

6. The random number generating method as claimed in claim 1, wherein

the random number formed by the signal

variation detecting circuit is used as an initial value of a random number generating circuit of the arithmetic method, and

a random number is generated by the random number generating circuit of the arithmetic method.

7. A random number generating method, wherein a signal of plural bits outputted from a plurality of unit circuits each having a first and a second logic circuit formed into an identical shape through an identical fabrication process and an amplifier circuit for forming a binary signal by amplifying a noise superposed on the differential voltage of threshold voltages of the first and the second logic circuits is transferred as an initial value to a random number generating circuit of the arithmetic method; and

a random number is generated from the random number generating circuit of the arithmetic method.

8. A semiconductor integrated circuit device comprising: a plurality of unit circuits each having a first and a second logic circuit formed into an identical shape through an identical fabrication process and an amplifier circuit for forming a binary signal by amplifying a noise superposed on the differential voltage of threshold voltages of the first and the second logic circuits; and

a signal variation detecting circuit for forming an output signal in response to variation in any of a plurality of binary signals outputted from the

plurality of unit circuits,

wherein a random number is generated from binary signal outputted from the signal variation detecting circuit.

9. The semiconductor integrated circuit device as claimed in claim 8, wherein

the first and the second logic circuit and the amplifier circuit are formed by logic gate circuits each having a first and a second input,

the first input and output of the logic gate circuit corresponding to the first logic circuit are connected,

the first input of the logic gate circuit corresponding to the second logic circuit is connected to the commonly connected input and output of the logic gate circuit corresponding to the first logic circuit,

an operation control signal is supplied to the second input of the logic gate circuit corresponding to the first and the second logic circuit,

the amplifier circuit includes a plurality of logic gate circuits whose first input and output are connected vertically, and the operation control signal is supplied to the second input.

10. The semiconductor integrated circuit device as claimed in claim 9, wherein the plurality of unit circuits are successively selected in response to an operation control signal formed by an order circuit,

and

the signal variation detecting circuit is arranged at the output unit of the plurality of unit circuits.

11. The semiconductor integrated circuit device as claimed in claim 9, wherein the signal variation detecting circuit includes an exclusive logic circuit for receiving output signals outputted from the order circuit so as to generate the random number.

12. The semiconductor integrated circuit device as claimed in claim 11, wherein the logic gate circuits are logic gate circuits of CMOS configuration and when the unit circuits are set to a non-active state by the operation control signal, P-channel MOSFET of the gate circuit of the next stage is set to an OFF state.

13. The semiconductor integrated circuit device as claimed in claim 11, wherein

the plurality of unit circuits are arranged in a matrix,

each of the unit circuits arranged in the matrix has an input unit having a logic gate circuit having a first input and a second input, a row and a column selecting signal are supplied to the first input and the second input, so that the output forms an operation control signal for setting the logic gate circuit constituting the first logic circuit and the second logic circuit to a selected state,

an output signal of a unit circuit of a

preceding stage arranged in the row direction is transmitted to the second input of the logic gate circuit constituting the amplifier circuit of each unit circuit and when the operation control signal is in a non-selected state, the amplifier circuit amplifies the output signal of the unit circuit of the preceding stage.

14. The semiconductor integrated circuit device as claimed in claim 11, wherein

the MOSFET constituting the unit circuit has a gate length and a gate width formed greater than a gate length and a gate width of the MOSFET constituting the other logic circuits containing the signal variation detecting circuit or the order circuit.

15. The semiconductor integrated circuit device as claimed in claim 11, wherein

the order circuit includes a test mode for selecting the same unit circuit a plurality of times continuously,

a circuit is provided for counting the number of unit circuits forming different outputs among the output signals outputted a plurality of times from the same unit circuit, and when the number of unit circuit forming the different output signals is one or more, the random number generating circuit is judge to have a high quality.